Production Technology for High-Yield, High-Performance GaAs Monolithic Amplifiers

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Abstract—**A production technology for GaAs MMIC's has been developed. In a six-month period, seventy 2-in wafers have been processed for *X*-band monolithic power and low-noise amplifiers and more than 2000 working chips have been produced. The two-stage power amplifiers have achieved a typical performance of 1.6-w output power with 8-dB associated gain and 20-percent power-added efficiency at 9.5 GHz. The two-stage low-noise amplifiers have consistently achieved 3-dB noise figure with 20-dB associated gain at the same frequency. Improvement of MMIC processing technology implemented in this work has resulted in an average dc chip yield of 15 percent.**

I. Introduction

ADVANCES IN GaAs material and wafer processing technologies in recent years have made the GaAs field effect transistor (FET) a very attractive device for applications at microwave and millimeter-wave frequencies. A GaAs FET is a far more versatile device than other two-terminal, solid-state devices such as Gunn diodes and IMPATT diodes in terms of application. Furthermore, since FET's are structurely very simple surface devices, they can be easily integrated with various passive circuit components in a monolithic configuration. A number of laboratories have demonstrated a variety of monolithic circuits with excellent microwave or millimeter-wave performance [1]–[6].

In order to implement these monolithic circuits in system applications, such as active phased-array antennas, space-borne communication systems, and electronic warfare (EW) systems, a production technology has to be developed to produce large quantities of "identical" and "affordable" chips. Unfortunately, progress on MMIC production has been very slow and very few papers addressing this important issue have been reported in the literature [7]. Recently, in order to transfer the technology from the laboratory into manufacturing, we have extensively investigated the producibility of MMIC's, using an *X*-band two-stage power amplifier and a two-stage low-noise amplifier as test vehicles for this study. The combination of optimum circuit design, proper material selection, batch wafer processing, and improved GaAs processing techniques has resulted in a reproducible, high-yield, high-performance MMIC production technology.

In this paper, the circuits design, material and processing improvements, and amplifier performance will be discussed. In addition, the fabrication yields for various components and the complete amplifier chips will be analyzed.

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II. Monolithic Circuit Design

A. Power Amplifier

The baseline approach for the monolithic power amplifier circuit design employs a single-ended, two-stage configuration. A 0.8×1500-μm gate power FET is used for the driver stage and two 0.8×1800-μm gate power FET's are used for the output stage. Fig. 1 shows the schematic of the power amplifier circuit design. A small-signal FET equivalent-circuit model was generated from the measured data of discrete FET's under low input power levels, and a large-signal model for the maximum output power was determined by load-pull measurement of the FET's. The large-signal model was used to synthesize a lossless output matching network; thus, maximum output power could be obtained from the matching circuit. The input and interstage networks were designed to provide gain flatness by utilizing the small-signal FET model. After the matching networks were synthesized, the SUPERCOMPACT program was used to optimize the final matching networks which consisted of all the microstrip transmission lines, discontinuities, and other passive components. Interdigital capacitors are used for the RF matching elements because they can be accurately controlled for small capacitance values. MOM overlay capacitors are used for RF bypassing and dc blocking because of their large capacitance per unit area. Airbridges are employed to interconnect the FET source pads and to connect the microstrip line to the top plate of the overlay capacitors. A substrate thickness of 0.1 mm is chosen to facilitate the fabrication of via holes. The use of via hole grounding allows greater flexibility in the layout of the amplifier because grounds can be placed almost anywhere on the circuit rather than only at the chip edges. In addition, it lowers source grounding inductance and reduces the time required to mount the chips. Fig. 2

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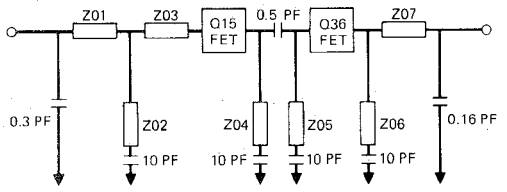

Q15 FET: INPUT FET (1500 um PERIPHERY)
Q36 FET: OUTPUT FET (3600 um PERIPHERY)

	Z01	Z02	Z03	Z04	Z05	Z06	Z07
WIDTH (μm)	66	66	33	66	66	66	66
LENGTH (μm)	497	311	87.3	633.3	246.7	678.7	1143

Fig. 1. Schematic of the two-stage power amplifier. This amplifier design consists of transmission-line and capacitor matching networks, and 0.8×1500-μm as well as 0.8×3600 μm FET's.

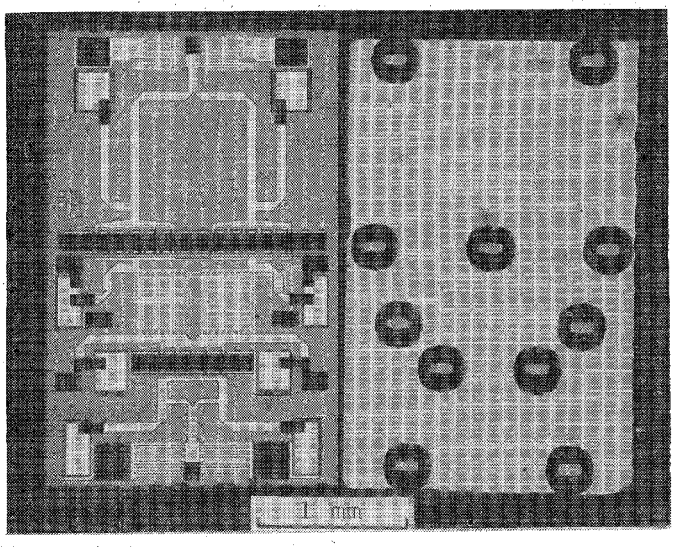

Fig. 2. Photographs of front and back sides of a complete power amplifier chip. This amplifier measures 2×3 mm and has thirty-four 0.8×150-μm gate fingers, eight 10-pF capacitors, twenty-seven airbridges, and eleven via holes.

shows the front and back sides of a finished power amplifier chip. There are thirty-four 0.8×150-μm fingers, eight 10-pf overlay capacitors, twenty-seven airbridges, and eleven via holes on each 2×3-mm power amplifier chip.

B. Low-Noise Amplifier

A single-ended, two-stage approach was chosen for the monolithic low-noise amplifier. Microstrip transmission lines are used for RF matching because of their low noise, low dispersion, and useful impedance range. The amplifier was designed using two 0.5×300-μm gate low-noise FET's. The FET equivalent-circuit model was generated from the measured S-parameters on discrete FET's and an in-house program was used to calculate the optimized noise model. The input matching network was synthesized to provide the optimum source impedance for minimum noise figure, while the interstage and output matching circuits were designed to provide the gain match. The circuit schematic for the low-noise amplifier is shown in Fig. 3, and the front and back sides of the low-noise amplifier chip are shown in Fig. 4. There are eight 0.5×75-μm gate fingers, five 10-pF overlay capacitors, nine airbridges, and five via holes on each chip.

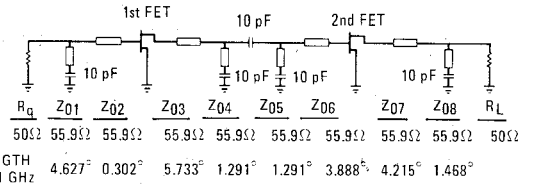

Fig. 3. Schematic of the two-stage low-noise amplifier. Standard 0.5×300-μm FET's are used in the design, and all the transmission lines and capacitors are suitable for MMIC realization.

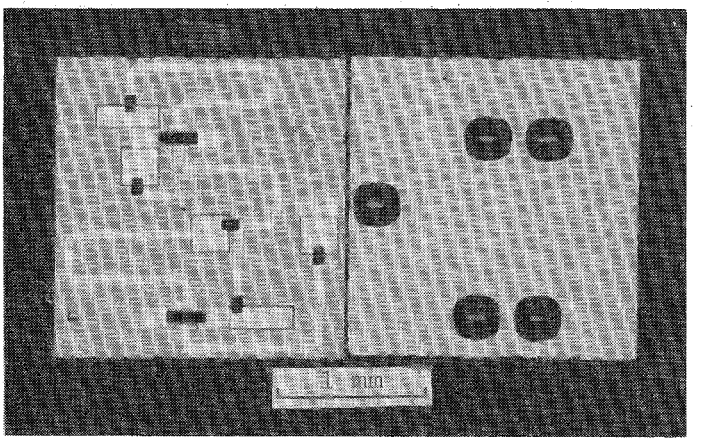

Fig. 4. Photograph of front and back sides of a completed LNA chip. This LNA has a dimension of 1.8×1.9 mm and has eight 0.5×75-μm gate fingers, five 10-pF capacitors, nine airbridges, and five via holes.

III. Material and Processing

The main objective of this work is to demonstrate the producibility, repeatability, and low-cost production of high-performance monolithic amplifiers. To accomplish this, we must select the optimum material and establish a high-yield, batch wafer process.

A. Material Selection

One of the major objectives of this task is to evaluate and select GaAs materials suitable for MMIC production. The principal selection criteria are: 1) amplifier performance, 2) uniformity, and 3) cost effectiveness.

Various GaAs materials including doped vapor phase epitaxy (VPE), ion implantation into the buffer layer, and direct ion implantation into semi-insulating substrates have been evaluated for both amplifiers. Direct ion implantation is the ultimately preferred approach due to the material cost, process flexibility (the ability to dope selectively), and on-wafer uniformity. However, the boule-to-boule and sometimes wafer-to-wafer inconsistency problems at present still hamper this technology for MMIC production. VPE materials, on the other hand, have demonstrated better wafer-to-wafer consistency and better device performance for both power and low-noise circuits. Therefore, in the early phase of this producibility study, we chose doped VPE materials for both amplifiers. The doping density (N)/active layer thickness (t) for the power and low-noise FET's are $1.2\times10^{17}\text{cm}^{-3}/4500$Å and $2.8\times10^{17}\text{cm}^{-3}/1800$ Å, respectively. The standard deviation of the $N\cdot t$ product distribution, as measured by source–drain current, is about 5 percent on a 2-in wafer and from wafer to wafer.

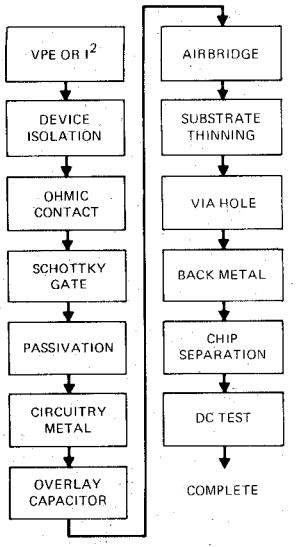

Fig. 5. Block diagram of MMIC fabrication procedure. The study identified that Schottky gate, passivation, overlay capacitor, and via hole fabrication are critical steps affecting MMIC yield and performance.

B. MMIC Processing

Batch processing is an important concept in simulating MMIC production conditions. We have tried batch processes with varying numbers of wafers per lot. On the basis of our present equipment and processes, six wafers per lot is the optimum size and has been chosen for this producibility study.

A block diagram of the MMIC fabrication procedure is given in Fig. 5. At the beginning of this study, the chip yield was about 5 percent, which was definitely too low for low-cost and high-volume production. Using process-monitoring test patterns, we were able to identify and later improve the critical steps that affected the MMIC yield and performance.

1) Schottky Gate: Excluding GaAs material, the Schottky gate is the most important element that determines the device performance and yield. The gate process includes definition by photolithography, recess etching, and metallization. Although *E*-beam lithography is capable of producing high-yield 0.5-μm gates, the optical approach was selected because of its higher throughput and more reliable equipment. We have developed a contact photolithography process capable of fabricating gates as small as 0.5 μm with high yield and consistency [2]. The SEM's in Fig. 6 show the 0.5-μm optical gates. Gate recess etching is a major cause of the spread of FET dc parameters (I_{DSS} and V_{PO}). By using controlled agitation and minimum etching steps (two to three steps), we were able to control the uniformity of I_{DSS}, after gate recess and metallization, to about 10 percent for the power amplifier and about 20 percent for the low-noise amplifier; the larger spread in the latter is due to the smaller photoresist opening. Gate metallization is another important factor that affects device performance and yield. Presently, Ti/Pt/Au is used for power amplifiers and Al is used for low-noise amplifiers for optimum yield and device performance.

2) Passivation: Protecting the MMIC circuit from mechanical and environmental damage and enhancing reliability require deposition of a passivation layer. The layer should have good physical integrity, a low surface state density at the interface with GaAs, low dielectric loss, and a low dielectric constant to function without impairing FET and circuit electric performance. Presently, our standard passivation material is a 2000 Å CVD SiO_2 film. The primary effect of the passivation is that the frequency response of the monolithic circuits shifts down by 500 MHz due to changes in the FET characteristics, whereas the output power, gain level, and noise figure of the amplifiers are preserved. This frequency shift can be corrected by using a revised FET model in the circuit design. Amplifier chips with this passivation have shown no performance degradation after subjected to a 135°C, 30 psi, and 100-percent humidity environment.

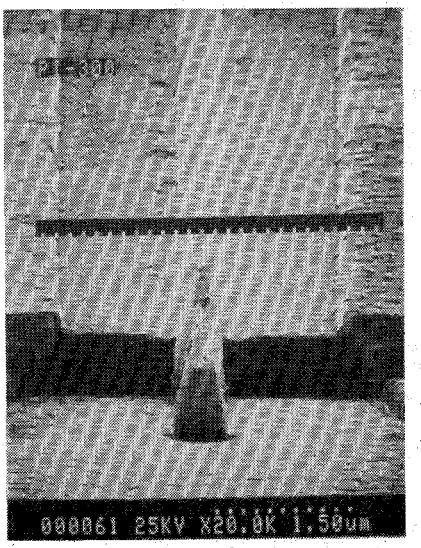

Fig. 6. SEM photographs of the 0.5-μm gates fabricated by optical photolithography. By using controlled agitation and minimum steps, we were able to fabricate these 0.5-μm gates with high yield and consistency.

3) Overlay Capacitor: MOM overlay capacitors are formed by sandwiching a 2500-Å sputter SiO_2 film between two metal layers. Capacitor failure due to pin holes in the dielectric film was identified as the major cause of low MMIC yield in the early lots. For the power amplifier

chip, achieving a 60-percent yield for the eight 10-pf capacitors requires the single capacitor yield to be better than $(0.6)^{1/8} = 0.94$ (94 percent). Subsequently, stringent control of wafer cleaning and handling, combined with the experimentally determined optimum SiO_2 thickness of 2500 Å, have resulted in consistently better than 95-percent yield for a 10-pf capacitor.

4) Via Hole: Via hole etching is the final step in the MMIC process. Wafers are first mounted device-side down on a lapping block and thinned to 100 μm. The surface is then coated with photoresist and the via hole pattern is aligned to the front circuit by using an IR mask aligner. The via holes are etched through the GaAs substrate with wet chemicals. Because of the nature of wet chemical etching, the size and uniformity of the via hole openings on the front surface are very sensitive to the exact wafer thickness and parallelism after thinning. Using the combination of a precision lapping and a chemical–mechanical polishing technique, 2-in GaAs wafers can be thinned down to 100 ± 5 μm with a mirror-finish and damage-free surface, which is the key to a high yield for via holes.

After implementing the process improvements described above, the chip yield has gradually increased to a healthy 15 percent.

IV. MMIC Yield

After the wafer processing is completed, individual MMIC chips are separated, visually inspected, and dc-tested. Visual inspection rejects chips with broken or shorted gates, incomplete or shorted circuits, over-etched via holes, surface contamination or defects, and edge cracks or chip-outs. The dc test measures the I_{DSS} and V_{PO} of the FET's, and tests for via hole connection and overlay capacitor shorts. DC acceptance criteria for the power FET's are I_{DSS}(FET 1) = 400 − 600 mA, I_{DSS} (FET 2) = 1000–1400 mA, and $V_{PO} \leqslant 6$ V. The criteria for low-noise FET's' are: I_{DSS} (FET 1 + FET 2) = 80 − 140 mA and $V_{PO} \leqslant 3$ V.

In a period of six months, seventy 2-in GaAs wafers have been processed and tested, and more than 2000 dc good-power and low-noise amplifier chips have been produced. The yield data have been accumulated and analyzed. On the power amplifier chip, the yield of the FET's with 5.1-mm total gate width is about 60 percent, the yield of the microstrip transmission lines and the interdigital capacitors is about 95 percent, the yield of eight overlay capacitors is about 60 percent, the yield of airbridges is about 95 percent, and the yield of via holes is about 90 percent. In addition, about 10 percent of the chips are lost from handling, edge effect, and dicing, and about 20 percent of the chips are rejected because the dc parameters (I_{DSS} and V_{PO}) fall outside of the specified windows. The best amplifier yield from a single 2-in wafer is close to 40 percent, the best yield from a 6-wafer lot is better than 25 percent, and the overall average yield is about 15 percent. This high chip yield was accomplished mainly by identifying and improving critical fabrication steps through batch processing a large number of wafers. Further yield improvement is expected when we continue on the learning curve for MMIC production.

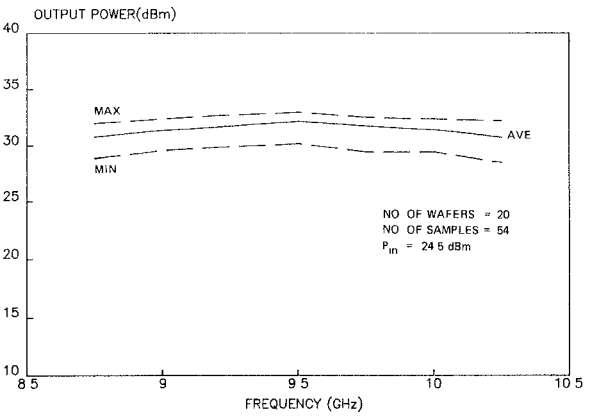

Fig. 7. Measured output power range of the monolithic power amplifiers. The measurement included 54 amplifier chips from 20 wafers, and was carried out at an input power of 24.5 dBm

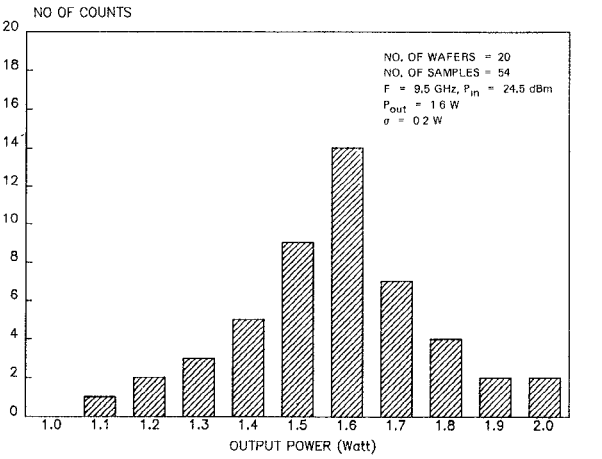

Fig. 8. Output power distribution of monolithic power amplifiers. Fifty-four amplifier chips from 20 wafers were measured, and a Gaussian distribution on the output power was observed.

V. Amplifier Performance

Three to five sample amplifier chips from each wafer were randomly selected from the dc-good chips, and mounted for RF evaluation. About 90 percent of the mounted devices are RF-functional, i.e., they have positive gain at *X*-band frequencies.

A. Power Amplifier

The typical small-signal gain of the power amplifier is 11 dB at 9.5 GHz. Output power is typically 1.6 W with 8-dB associated gain and 20-percent power-added efficiency. The best output power is 2 W with 8.5-dB gain and 25-percent power-added efficiency at 9.5 GHz. The range of output power of 54 amplifier chips from 20 different wafers is shown in Fig. 7. A histogram of the distribution from the same samples is given in Fig. 8.

The phase tracking of the power amplifiers have also been tested. The variation of the phase angle of the large signal S_{21} is approximately 7 degrees from chip to chip on the same wafer, and is approximately 18 degrees from wafer to wafer.

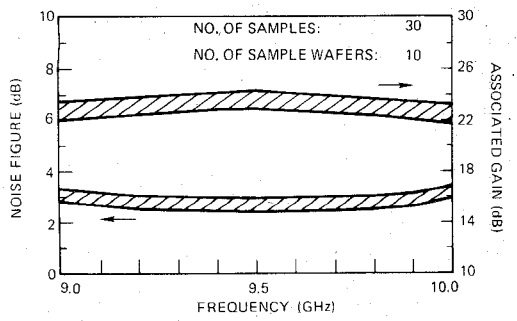

Fig. 9. Measured gain and noise figure ranges of monolithic LNA's. The measurement included 30 LNA's from 10 wafers, and showed ±0.8-dB and ±0.3-dB variations in gain and noise figure, respectively.

B. Low-Noise Amplifier

Sample low-noise amplifier chips have been measured and the gain–noise figure curves of 30 amplifiers from 10 different wafers are shown in Fig. 9. The typical noise figure is 3 dB with 20-dB associated gain across the 1-GHz bandwidth.

VI. Conclusion

Combining the choice of optimum material, refined processing techniques, and relaxing the constraints of circuit design, a production technology for high-yield and high-performance MMIC's has been developed and demonstrated. Improvement of MMIC processing technology has resulted in an average chip yield of 15 percent over 70 processed wafers. Two-stage *X*-band power amplifiers deliver a typical output power of 1.6 W with 8-dB associated gain and 20-percent power-added efficiency. Low-noise amplifiers have typical performance of 3-dB noise figure with 20-dB associated gain. This work has demonstrated the feasibility of producing the large quantities of MMIC chips. Based on this experience, we believe that GaAs MMIC's are ready for production. Further refinement of the design and processing will result in low-cost MMIC chips in the near future.

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References

[1] D. M. Maki, J. M. Schellenberg, H. Yamasaki, and L. C. T. Liu, "A 69 GHz monolithic FET oscillator," in *Dig. 1984 IEEE Microwave and Millimeter-Wave Monolithic Circuit Symp.* May 1984, pp. 62–66.

[2] L. C. T. Liu, D. W. Maki, C. Storment, M. Sokolich, and W. Klatskin, "An 8–18 GHz monolithic two-stage low noise amplifier," in *Dig. 1984 IEEE Microwave and Millimeter-Wave Monolithic circuit Symp.*, May 1984, pp. 49–51.

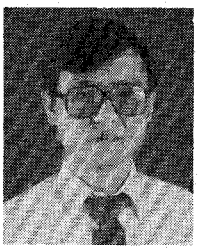
[3] M. C. Driver, S. K. Wang, J. X. Przybysz, V. L. Wrick, R. A. Wickstrom, E. S. Coleman, and J. G. Oakes, "Monolithic microwave amplifiers formed by ion implantation into LEC GaAs substrates," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 191–196, Feb. 1981.

[4] Y. Ayasli, S. M. Miller, R. Mozzi, and L. K. Hanes, "Capacitively coupled traveling-wave power amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 1704–1709, Dec. 1984.

[5] S. B. Moghe, H-J. Sun, T. Andrade, C. C. Huang, and R. Goyal, "A monolithic direct-coupled GaAs IC amplifier with 12-GHz bandwidth," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 1698–1703, Dec. 1984.

[6] S. Hari, K. Kamei, K. Shibata, M. Tatematsu, K. Mishima, and S. Okano, "GaAs MMIc's for direct broadcast satellite receivers," vol. MTT-31, pp. 1089–1096, Dec. 1983.

[7] D. N. McQuiddy, Jr., J. W. Wassel, J. B. Lagrange, and W. R. Wisseman, "Monolithic Integrated Circuits: A Historical Perspective," vol. MTT-32, pp. 997–1008, Sept. 1984.



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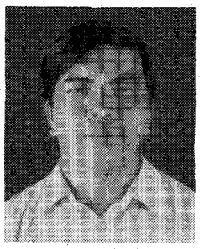
He joined Hughes Aircraft Company, Torrance Research Center, in 1983, where he is currently head of the Microwave Devices Development Section, responsible for the development of GaAs FET devices and MMIC fabrication technology. Prior to joining Hughes, he was a Senior Engineer at Westinghouse Research Center at Pittsburgh, PA. There he was involved with GaAs Material Processing, device modeling, and monolithic IC fabrication technology.



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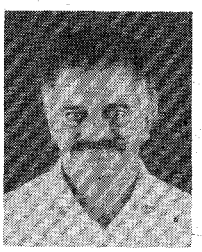
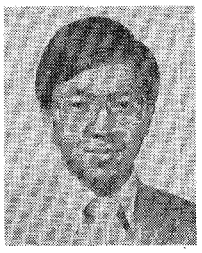


Mario Siracusa was born in Brooklyn, NY, on September 16, 1934. He received the A.A. degree in electrical engineering from Santa Ana College, Santa Ana, CA.

He has been involved in semiconductor processing for over 25 years. In 1959, he joined Hughes Aircraft Company. He was involved in the processing and device development of 1-GHz Ge transistor, thin-film FET devices, Si IMPATT diodes, p-i-n diodes, millimeter-wave GaAs varactor diodes. In 1974, he was responsible for developing and setting up of GaAs FET processing capability at Torrance Research Center. At present, he is Head of GaAs processing of GaAs devices and monolithic integrated circuits at TRC.



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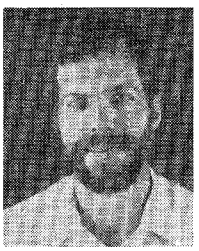
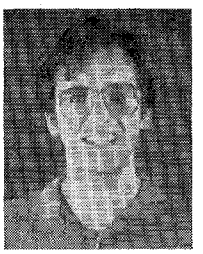


Robert G. Pauley received the B.S. degree in electrical engineering (1982) and the M.S. degree in electrical engineering (1984) from the Georgia Institute of Technology. His studies there concentrated on communication theory and electromagnetics.

In 1982, he was a research engineer at Georgia Tech's Engineering Experiment Station, where he was involved in millimeter-wave radar design. In 1984, he joined Hughes Aircraft Company's Torrance Research Center to work on monolithic GaAs IC's. His work there includes the design and evaluation of MMIC components and circuits.



Peter Asher received the Bachelor's degree in chemical engineering from the University of California at Berkeley in 1979. He then joined Hughes and worked on GaAs IMPATT and mixer diodes. Since then he has worked on GaAs field effect transistors and GaAs monolithic microwave integrated circuits.

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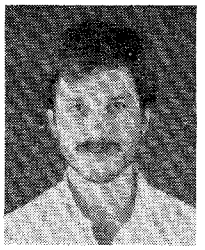

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Since 1982, he has been a member of the technical staff at the Torrance Research Center of Hughes Aircraft Company. His primary research interests have focused on the development of advanced process techniques for high-speed GaAs digital circuits and MMIC's. Specific areas of research include: GaAs digital IC producibility, dielectrics for passivation and device application, dry etching, thin-film resistors, process modeling, and enhancement-mode FET development.

Mr. Sokolich is a member of the American Vacuum Society.